TNG-4 Streaming Protocol

Dave has decreed that for the Sandia QuadPod Project, TNG-4 shall stream its data. This is problematic if analog data resolution in excess of 8 bits is required, as the TNG-4 streaming protocol has not been expanded to accommodate the extended resolution.

The command-mode protocol does support the extended ADC resolution. Moreover, the host program can change the resolution with TNG-4s populated with PIC processors capable of the extended ADC resolution. The downside is that the command-mode TNG-4 has to be continuously asked for its data, and the extended resolution is not the default condition. Extended resolution has to be set.

For fear that a TNG-4 would not send data (or the correct data) because of some lapse in communications or protocol, Dave has made the requirement that these boxes just power-up and start sending data.

This may be unwise in a USB environment, because TNG-4 now becomes a bandwidth hog, particularly when turbocharged to 57.6 kbps.

In any event, I'm presenting here my proposal for an extended TNG-4 streaming protocol. For the sake of clarity and history, I've documented the first two major versions for comparison.

Implementation of this new protocol will require modification of the existing NeatTools TNG-4 module in addition to modifications to the TNG-4 firmware.

Please comment.

The Original TNG-4 Streaming-mode Protocol:

From TNG-4:
Separator Byte: AAh (10101010) alternating with 55h (01010101).
Analog Channel 1 (8-bits)
Analog Channel 2
Analog Channel 3
Analog Channel 4
Analog Channel 5
Analog Channel 6
Analog Channel 7
Analog Channel 8
B-Port Digital Data
C-Port Digital Data
D-Port Digital Data

[19.2k baud data rate, 12 bytes/packet. Therefore, 160 packets/second (maximum).]

To TNG-4:
Separator Byte: A5h (10100101) alternating with 5Ah (01011010).

Attribute Byte:

7	6	5	4	3	2	1	0
D4	D3	D2	D1	0	D	C	B

If B-bit =1: "B" (42h)
B-Port Configuration Byte (bit = 1 for input, 0 for output)
B-Port Output Data (masked by configuration byte)

If C-bit=1: "C" (43h)
C-Port Configuration Byte
C-Port Output Data

If D-bit=1: "D" (44h)
D-Port Configuration Byte
D-Port Output Data

Port C bit 0 = test switch (input)
Port C bit 1 = DAC enable line (output)
Port C bit 3 = SPI clock (output)
Port C bit 4 = SPI data in (input)
Port C bit 5 = SPI data out (output)
Port C bit 6 = RS-232 data out (output)
Port C bit 7 = RS-232 data in (input)

If (D1 or D2 or D3 or D4 = 1): "A" (41h)

If (D1 = 1): DAC Channel 1 Value
If (D2 = 1): DAC Channel 2 Value
If (D3 = 1): DAC Channel 3 Value
If (D4 = 1): DAC Channel 4 Value

Only sections with new data are sent as per the attribute byte. The minimum packet size is two bytes. The maximum packet size is 16 bytes.

The maximum rate that one digital port could be changed is (19.2 kbps=1920 bytes per second / 5 bytes = 384 Hz). Similarly, the maximum rate that one DAC channel could be changed would be 480 Hz. All four DAC channels can be updated at 274 Hz.

Latest TNG-4 SPI Streaming-mode Protocol (4/2003):

This protocol replaces all the current SPI protocols and is **not** backwards-compatible with previous SPI protocols.

1. The attribute byte (2nd byte) of the streaming protocol is modified such that the currently unused bit would be used to signify that SPI information is part of the packet, thusly:

7	6	5	4	3	2	1	0
D4	D3	D2	D1	S	D	C	B

Attribute Byte: S=1 if SPI information is attached; otherwise = 0.

2. If S-bit=1: “S” (53h) followed by an SPI flag byte and 1-31 SPI data bytes. The SPI Flag Byte = 0 if no SPI data follows; otherwise:

7	6	5	4	3	2	1	0
R/W	S2	S1	S0	CM	D2	D1	D0

R/W: This bit = 0 when data is output only.
This bit = 1 when reading data.

S2-S0: These bits specify which SPI enable line to use.
000 = Port C bit 2
001 = Port D bit 7
010 = Port D bit 6
011 = Port D bit 5
100 = Port D bit 4
101 = Port D bit 3
110 = Port D bit 2
111 = Port D bit 1

CM: This bit=ON causes a reinterpretation of the SPI flag byte. No SPI data is sent, and the next byte in the stack is expected to be another SPI flag byte (or 0).

With CM=1 The SPI flag byte is interpreted as:

7	6	5	4	3	2	1	0
SMP	CKE	---	CKP	1	---	SSPM1	SSPM0

SMP = SSPSTAT:SMP bit for PIC with same meaning.
0 = Input sampled at end of output (default).
1 = Input sampled in middle of output bit.

CKE = SSPSTAT:CKE bit for PIC with same meaning.
0 = Data output on leading edge of clock.
1 = Data output on trailing edge of clock (default).

CKP = SSPCON:CKP bit for PIC with same meaning.
0 = Clock normally low (default).
1 = Clock normally high.

SSPM1 and SSPM0 set the clock rate.
00=FOSC/4 (1MHz, default)
01=FOSC/16 (250kHz).
10=FOSC/64 (62.5kHz).
11=undefined (don’t do it!).

This command redefines SPI operations until the next SPI configuration byte is received or TNG-4 is power-cycled.

Please note that the DAC is an SPI device and that changes to SPI function may adversely affect the operation of the built-in DAC.

D2-D0: These bits specify the number of data bytes to send/receive (1-7). If D2-D0 = 7 the next byte in the sequence will be interpreted as the number of SPI bytes to send and/or receive. If the byte is 0, no bytes are sent. Do not exceed 31 bytes!

This protocol will support MAX3100/3110 operations if you do the initialization yourself, and send two bytes where the first byte is always 080h.

3. When requesting that SPI-data be read back, after the normal outgoing data stream completes transmission and SPI data is being sent, TNG-4 will send a 0FFh byte instead of the separator character. SPI data will be returned in the same form and order that it was requested including the SPI-flag bytes.

   The following is an example:

   From computer: A5 08 53 92 xx yy

   This says send an SPI message. The message is two bytes (xx and yy) using Port D bit 7 as the enable line and which should return SPI data.

   From TNG-4: AA a1 a2 a3 a4 a5 a6 a7 a8 bd cd dd ED e0 e1 e2 e3 FF 92 xx yy

   This message is the usual 8 analog channels (a1-a8) and digital I/O ports (bd, cd, and dd) followed by extended resolution A/D data bytes and the returned SPI data.

New Extended-Resolution TNG-4 Streaming-mode Protocol: (proposed 5/14/2003)

PIC microcontrollers are available that support 10 and 12-bit ADC resolutions (for example, PIC16F874 (10-bit) and PIC16C774 (12-bits). These processors also run at clock speeds of up to 20 MHz.

The extended-resolution ADC microcontrollers support left- or right-justifying the ADC result in 2 byte-wide registers. This protocol will use the left-justified format. If the bits are left justified in the word, the receiver doesn't have to make distinctions between the two extended bit resolutions when mapping the ADC result to voltage.

There will be no mechanism (at this time) for changing the ADC resolution. A TNG-4 will use 8-bit, 10-bit, or 12-bit ADC resolution depending on the processor installed in the TNG-4.

The first change from the TNG-4 SPI protocol is the separator byte. The 10- or 12-bit version of TNG-4 will utilize that same pair of separator bytes for both incoming and outgoing data streams. This is a change from the AAh/55h separator for 8-bit TNG-4s.

The second change is the addition of 4 extra bytes in the data packets from TNG-4. These 4 bytes contain the packed least significant bits for the 8 ADC channels. The least significant bits for an ADC channel (2 or 4::10-bits or 12-bits) are left-justified in the nibble corresponding to that channel. Odd-numbered channels (when counting from 1) are located in the upper nibble (bits 4-7); even-numbered channels are located in the lower nibble (bits 0-3).

From TNG-4:

Separator Byte: A5h (10100101) alternating with 5Ah (01011010).
Analog Channel 1 Most significant byte (MSB): 8-bits
Analog Channel 2 MSB
Analog Channel 3 MSB
Analog Channel 4 MSB
Analog Channel 5 MSB
Analog Channel 6 MSB
Analog Channel 7 MSB
Analog Channel 8 MSB
Analog Channel 1 and 2 Least significant bits (LSB) combined into one byte
Analog Channel 3 and 4 LSB
Analog Channel 5 and 6 LSB
Analog Channel 7 and 8 LSB
B-Port Digital Data
C-Port Digital Data
D-Port Digital Data

[57.6 kbps data rate, 16 bytes/packet. Therefore, 360 packets/second (maximum).]

To TNG-4:

Separator Byte: A5h (10100101) alternating with 5Ah (01011010).

Attribute Byte:

7	6	5	4	3	2	1	0
D4	D3	D2	D1	S	D	C	B

If B-bit =1: "B" (42h)
B-Port Configuration Byte (bit = 1 for input, 0 for output)
B-Port Output Data (masked by configuration byte)

If C-bit=1: "C" (43h)
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If D-bit=1: "D" (44h)
D-Port Configuration Byte
D-Port Output Data

Port C bit 0 = test switch (input)
Port C bit 1 = DAC enable line (output)
Port C bit 3 = SPI clock (output)
Port C bit 4 = SPI data in (input)
Port C bit 5 = SPI data out (output)
Port C bit 6 = RS-232 data out (output)
Port C bit 7 = RS-232 data in (input)

If (D1 or D2 or D3 or D4 = 1): “A” (41h)

If (D1 = 1): DAC Channel 1 Value
If (D2 = 1): DAC Channel 2 Value
If (D3 = 1): DAC Channel 3 Value
If (D4 = 1): DAC Channel 4 Value

S=1 if SPI information is attached; otherwise = 0.

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Please note that the DAC is an SPI device and that changes to SPI function may adversely affect the operation of the built-in DAC.

D2-D0: These bits specify the number of data bytes to send/receive (1-7). If D2-D0 = 7 the next byte in the sequence will be interpreted as the number of SPI bytes to send and/or receive. If the byte is 0, no bytes are sent. Do not exceed 31 bytes!

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